REMARKS

At the time of the Office Action dated June 7, 2005, claims 2-4, 6-9, 11-17, 19-26, 55-62 and 75-79 were pending in this application. Applicant acknowledges, with appreciation, the Examiner's allowance of claims 8, 9, 12, 22-26, 55-62 and 75-78.

In this Amendment, claims 3 and 15 have been amended for clarification, and claim 2 canceled. Care has been exercised to avoid the introduction of new matter. The amendment of the claims does not narrow the claimed scope for any reason relating to patentability.

Applicants also acknowledge, with appreciation, Examiner Nguyen's courtesy and professionalism in conducting a telephonic interview on June 28, 2005, during which the reason of the rejection of the claims was discussed.

Claims 13 and 14 have been rejected under 35 U.S.C. §112, second paragraph.

The Examiner generally asserted that claims 13 and 14 are not supported in the specification and indefinite. In response, Applicant believes that the recitations at issue have been well-known and that a person skilled in the art does not need the specific description thereof.

With respect to claim 13, the Examiner specifically asserted that the recitation "at least one of a power supply potential and a ground potential of said buffer circuit varies using a control signal" renders the claim indefinite since it is not clear how one of a power supply potential and a ground potential of the buffer circuit varies (using a control signal)." The Examiner further stated, "according to Figures 1 and 7 of the claimed invention, there is no control signal shown that would provide variations in either the power supply potential or the ground potential." See paragraph 2 of the Office Action.

Applicant notes that the claimed technology is implemented in such devices as "LongRun2" of Transmeta Corporation and "Extended Intel SpeedStep®" in Pentium® M of Intel Corporation.

In particular, when the above technology is applied inside a LSI, a transistor for voltage control is inserted between power supply/ground and a relevant gate. On the other hand, when the above technology is externally applied to a LSI, an another approach is taken with a regulator. Voltage control regulator, for example, the regulators with VRM specification of Intel Corporation, are widely distributed in the market.

For claim 14, the Examiner asserted, "the recitation 'a substrate potential of a transistor included in said buffer circuit varies using a control signal' renders the claim indefinite since it is not clear how a substrate potential of a transistor included in said buffer circuit varies using a control signal (using a control signal)." The Examiner further asserted, "according to Figures 1 and 7 of the claimed invention, there is no control signal shown that would provide variations in the substrate potential." See paragraph 2 of the Office Action.

As for the substrate potential control in claim 14, this technology has been used in the VT-CMOS technology and others. Controlling the threshold voltage Vth by varying the substrate voltage is described, for example, by T. Kuroda, et al., "A 0.9V 150 MHz 10mW 4mm^2 2-D discrete cosine transform core processor with variable-threshold-voltage scheme," IEEE J. Solid-State Circuits, 31, (11), pp. 1770-1779, Nov. 1996.

The VT-CMOS technology is directed to strike a balance between low leak current and fast switching, and therefore, the object thereof is totally different from that of the subject application. The method to control the substrate potential itself is, however, almost the same as claim 14. In the VT-CMOS technology, although it is common that a substrate voltage is generated in a LSI as described in the above Kuroda reference, it is also possible to control a substrate potential by controlling a regulator out of a LSI. Voltage control regulators, e.g., the regulators with VRM specification of Intel Corporation, are widely distributed in the market.

It is noted that the above conventional technologies are employed to control the power supply/ground potential in a whole LSI or a large module unit, which are basically different from the claimed invention of controlling some specific gates. Additionally, the object of the above conventional technologies is either to lower the power supply voltage or to raise the threshold voltage, which is fundamentally different from that of the claimed invention to control the duty ratio of the clock signal.

Based on the foregoing, claims 13 and 14 are definite, and withdrawal of the rejection of the claims is respectfully solicited.

Claims 13 and 14 have been rejected under 35 U.S.C. §102(e) as being anticipated by Yen.

It is noted that claims 13 and 14 are definite for the reasons set forth above.

For claim 13, the Examiner asserted, among other things, that Yen discloses "at least one of a power supply potential and a ground potential of said buffer circuit varies using a control signal" because of control signals CTL1 and CTL2 in Fig. 7A of Yen.

Yen describes control signals CTL1 and CTL2 as follows:

> Counter-sequencer 34 drives first control signal CTL1 to the gate of load-switching transistor 26, and second control signal CTL2 to the gate of second load-switching transistor 36. When CTL1 is high, capacitor 28 has to be charged and discharged by input buffer 22 before the logic threshold of output buffer 24 is reached, thus delaying clock edges. When CTL2 is high, capacitor 38 has to be charged and discharged by input buffer 22 before the logic threshold of output buffer 24 is reached, thus also delaying clock edges. When both CTL1 and CLT2

> are high, both capacitors 28, 38 have to be charged, further delaying clock edges. See column 6, lines 33-45.

It is apparent that the above portion describes varying control signals CTL1 and CTL2, but does not disclose varying "at least one of a power supply potential and a ground potential of said buffer circuit" by a control signal.

With respect to claim 14, the Examiner further asserted that control signals CTL1 and CTL2 describes "a substrate potential of a transistor included in said buffer circuit varies using a control signal." In response, as discussed above, Yen discloses varying control signals CTL1 and CTL2 to control gates of transistor 26, 36, whereas the claimed invention requires varying a power supply potential or a ground potential of a buffer circuit.

Accordingly, it is submitted that the claimed invention is different from what is disclosed in Yen, and thus the reference does not identically disclose a clock generation circuit including all the limitations recited in claims 13 and 14. Withdrawal of the rejection of the claims is respectfully solicited.

Claims 15 and 16 have been rejected under 35 U.S.C. §102(b) as being anticipated by Yamato et al.; and claim 17 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Yamato et al.

With respect to independent claim 15, the Examiner asserted that Figs. 2, 3A and 3B of Yamato et al. disclose what is claimed in claim 15: a PLL 46, an internal clock generation portion 200 and buffers 47-19, a delay device 40, and an AND device 44 correspond to the claimed frequency-multiplying circuit, buffering portion, delay circuit and logic element.

In response, it is submitted that Yamato et al. does not disclose using a delay control signal to control a delay time of the delay circuit. For example, delay devices 502, 503 in Fig.

3A of Yamato et al. do not receive any control signal to control a delay time. It is also submitted that dependent claims 16 and 17 are patentably distinguishable at least because they respectively include all the limitations of independent claim 15.

Accordingly, Yamato et al. does not disclose or teach all the limitations recited in claims 15-17. Withdrawal of the rejection of the claims is respectfully solicited.

Claims 2-4 and 11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yen in view of Proebsting.

It is noted that the rejection of claim 2 has been rendered moot by cancellation of the claim.

With respect to claim 3, the Examiner admitted that Yen fails to disclose, among other things, that "at least one of a power supply potential or a ground potential in said buffer circuit is different from another power supply voltage or ground voltage in said buffer portion." However, the Examiner applied Proebsting and asserted that the reference teaches the missing feature. The Examiner, then, concluded that it would have been obvious to modify Yen's circuit based on the teachings of Proebsting to arrive at the claimed invention. This rejection is respectfully traversed.

In response, it is submitted that the Examiner did not provide where Proebsting teaches the limitation "at least one of a power supply potential or a ground potential in said buffer circuit is different from another power supply voltage or ground voltage in said buffer portion." Applicant reviewed Proebsting, and stresses that at least Fig. 1B of Proebsting, cited by the Examiner, does not even refer to a power supply voltage.

In the interview, the Examiner asserted the limitation is inherent because the limitation can be read as follows: a power supply potential in said buffer circuit is different from another ground voltage in said buffer portion." However, in this Amendment, the limitation in claim 3 has been amended as follows "at least one of a power supply potential or a ground potential in said buffer circuit is different from another power supply voltage or ground voltage, respectively, in said buffering portion." For a person skilled in the art, it would have been apparent that original claim 3 intended to recite the limitation in the amended manner. Accordingly, Applicant submits that Proebsting does not teach the above limitation.

It is, therefore, submitted that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis. Withdrawal of the rejection of claim 3 is respectfully solicited.

For claim 4, the Examiner asserted that "due to the difference in the transistor sizes," the limitation "a substrate potential of a transistor included in said buffer circuit is different from a substrate potential of another transistor included in said buffering portion" is obvious (see page 8, the second full paragraph, in the Office Action).

First, Applicant submits that the Examiner did nor provide where Proebsting teaches the limitation "a substrate potential of a transistor included in said buffer circuit is different from a substrate potential of another transistor included in said buffering portion," recited in claim 4. Based on Applicant's review of the reference, at least Fig. 1B of Proebsting (cited by the Examiner) does not even refer to a substrate potential, since all of the transistors in Fig. 1B are depicted as three-terminal (gate, source and drain) ones and having no backgate.

Second, the Examiner's assertion that the above limitation is obvious "due to the difference in the transistor sizes" is simply the generality. On the contrary, in the above limitation in claim 4, the difference between "a substrate potential of a transistor included in said buffer circuit" and "a substrate potential of another transistor included in said buffering portion" is clearly intended to recite that a logic low period and a logic high period of the clock signal are different from each other.

Accordingly, Proebsting does not teach the claimed invention in claim 4. It is, therefore, submitted that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis. Withdrawal of the rejection of claim 4 is respectfully solicited.

With respect to claim 11, the Examiner asserted that Proebsting discloses a driving capability control portion recited in claim 11. Applicant responds that Proebsting does not teach anything about at least the driving capability control portion of claim 11 for the reasons set forth below.

Fig. 1B of Proebsting discloses a plurality of buffers connected in series. In contrast, Figs. 4-6 of the present application discloses a plurality of buffers connected in parallel. A plurality of buffers must be connected in parallel as depicted in Figs. 4-6 of the subject application to change the driving capability. Therefore, the circuit depicted in Fig. 1B of Proebsting cannot change the driving capability, whereas the driving capability control portion of claim 11 can do so.

Therefore, the applied combination of Yen and Proebsting does not teach or suggest a clock generation circuit including all the limitations recited in claim 11. Specifically, the references do not teach a driving capability control portion recited in claim 11. Withdrawal of the rejection of the claim is respectfully solicited.

Claims 6 and 19-21 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yen in view of Lane.

In the statement of the rejection, the Examiner admitted that Yen fails to teach, among other things, "a counter determining a digital count value based on a phase comparison result output from said comparator," recited in independent claims 6 and 19. However, the Examiner asserted that counter 24 in Lane corresponds to the claimed counter.

However, Lane's counter 24 and the claimed counter are different from each other. Lane's counter is "loaded with an initial count value which is used to determine how many cycles of the output clock signal 13 are to be generated for each cycle of the reference clock signal 1" (column 2, line 65 to column 3, line 2). On the other hand, the claimed counter determines a digital count value based on a phase comparison result from a comparator. The applied combination of Yen and Lane does not teach a counter using a phase comparison result from a comparator.

Based on the forgoing, it is submitted that the applied combination of Yen and Lane does not teach and suggest all the limitations recited in independent claims 6 and 19. Dependent claims 20 and 21 are also patentably distinguishable at least because those claims include all the limitations recited in independent claim 19. Applicant, therefore, respectfully solicit withdrawal of the rejection of claims 6 and 19-21, and favorable consideration thereof.

Claims 7 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Yen in view of Suda.

In the statement of the rejection, the Examiner admitted that Yen fails to teach a ring oscillator including a comparator, a counter, first and second delay lines and a selector, recited in claim 7. However, the Examiner applied Suda, and asserted that the reference teaches missing features. The Examiner then concluded that it would have been obvious to modify Yen's circuit based on the teachings of Suda to arrive at the claimed invention.

Fig. 16 of Suda describes a delay line (a portion of circuits constituting a DLL) controlled by a general counter. The delay line generates a delay in response to the counter value. Counter 73 and delay lines 74, 75 in Fig. 17 of the present application corresponds to the circuit shown in Fig. 16 of Suda.

However, Fig. 16 of Suda does not teach the claimed selector to control the duty ratio, i.e., "a logic high period and a logic low period different from each other," by "selecting and outputting an input from one of said first and second delay lines," recited in claim 7.

Accordingly, the applied combination of Yen and Suda does not teach or suggest all the limitations recited in claim 7. Withdrawal of the rejection is respectfully solicited.

Claim 79 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Proebsting in view of Lane.

In the statement of the rejection, the Examiner admitted that Proebsting fails to disclose, among other things, a counter determining a digital count value based on a phase comparison result from said comparator," recited in claim 79. However, the Examiner applied Lane, and asserted that the reference teaches the limitation.

However, as discussed for the rejection of claims 6 and 19-21, Lane does not teach the claimed counter, because Lane's counter is configured not to use a result of the comparator. Accordingly, it is submitted that the applied combination of Proebsting and Lane does not teach a clock generation circuit including all the limitations recited in claim 79. Applicant, therefore, respectfully solicits withdrawal of the rejection of claim 79 and favorable consideration thereof.

Conclusion.

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Recognition under 37 C.F.R. 10.9(b)

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